REMARKS

This is intended as a full and complete response to the Final Office Action dated October 3, 2006, having a shortened statutory period for response set to expire on January 3, 2007. Please reconsider the claims pending in the application for at least the reasons discussed below.

Claims 1, 3-12, 14-19, and 21-26 remain pending in the application. Claims 1, 3-12, 14-19, and 21-26 are rejected. Reconsideration of the rejection of claims 19 and 21-26 is requested for the reasons presented below.

Applicants propose canceling claims 1, 3-12, and 14-18. Applicants propose amending claim 19 to clarify that "depositing a metal-containing layer on the substrate to fill the vertical interconnect and the horizontal interconnect" refers to depositing a metal-containing layer that fills both a vertical interconnect and a horizontal interconnect. Applicants submit that the proposed amendment to claim 19 does not raise new issues, as claim 19 already recites a method of forming a dual damascene structure, which inherently includes depositing a metal-containing layer that fills both a vertical interconnect and a horizontal interconnect. Applicants submit that the changes proposed herein reduce the issues for appeal and do not introduce new matter. Applicants respectfully request entry of the proposed amendments.

Claims 1, 3-12, and 14-18 are rejected under 35 U.S.C. § 103(a) as being unpatentable over *Yang, et al.* (U.S. Patent No. 6,734,559) in view of *Gates, et al.* (U.S. Patent No. 6,203,613). Applicants submit that the rejection of claims 1, 3-12, and 14-18 is rendered moot as Applicants propose canceling claims 1, 3-12, and 14-18.

Claims 19 and 21-26 are rejected under 35 U.S.C. § 103(a) as being unpatentable over *Yang, et al.* in view of *Gates, et al.*, and further in view of *Naik, et al.* (U.S. Patent No. 6,204,168). Applicants respectfully traverse the rejection.

In the Advisory Action mailed December 18, 2006, the Examiner states that Applicants argued in the previously filed Response to Final Office Action dated October 3, 2006, that *Yang, et al.* in view of *Gates, et al.* would not be successfully combined with *Naik, et al.* because the final structure of *Yang, et al.* discloses a dual damascene in which the interconnects are separated by a barrier layer and seed layer. Applicants

respectfully submit that while the previously filed Response to Final Office Action dated October 3, 2006, states "there is no reasonable expectation of success for using *Naik, et al.'s* dual damascene process in which a metal layer simultaneously fills both a vertical interconnect and a horizontal interconnect (column 7, lines 4-14 of *Naik, et al.*) to form the structure of *Yang, et al.*, as the interconnects of *Yang, et al.* are separated by a barrier layer and a seed layer", Applicants did not state that the final structure of *Yang, et al.* discloses a dual damascene (emphasis added by Applicants) in which the interconnects are separated by a barrier layer and seed layer. While the Examiner states in the Final Office Action dated October 3, 2006, that *Yang, et al.* in view of *Gates, et al.* teaches a method of forming a dual damascene structure comprising etching a second dielectric film to define a horizontal interconnect and a vertical interconnect and depositing a metal-containing layer on the substrate to fill the vertical interconnect and the horizontal interconnect (*Yang, et al.*, Figure 3, 201, 210), Applicants respectfully submit that *Yang, et al.* in view of *Gates, et al.* provides two single damascene layers and does not provide a dual damascene structure for interconnects 201 and 210.

Yang, et al. discloses that the structure of Figure 3 is formed through the steps of depositing conductive material in the channel 201 using the first damascene process described therein with respect to Figures 1 and 2 (column 5, lines 40-45). In the first damascene process, a channel opening 125 is defined in a channel dielectric 126 above the via 110 and dielectric layer 112. *Yang, et al.* does not teach or suggest etching the channel dielectric 126 and also continuing to etch an exposed dielectric layer 112 to define the via 110. Thus, *Yang, et al.* does not teach or suggest that the formation of the channel opening 125 is part of a dual damascene opening process.

After the channel opening 125 is formed, the channel opening 125 is then filled with a barrier, seed, and metal layer (column 4, lines 49-60). *Yang, et al.* does not teach or suggest that filling of the channel opening 125 also fills the channel 110, and thus, does not teach or suggest that the filling of the channel opening 125 is part of a dual damascene process. Instead, *Yang, et al.* provides a single damascene process for forming channel opening 125 and channel 101, and thus also provides a single damascene process and single damascene structure for channel 201.

Applicants further submit that there is no reasonable expectation of success for using a dual damascene process in which a metal layer simultaneously fills both a vertical interconnect and a horizontal interconnect to form the interconnects 201 and 210 of the structure of *Yang, et al.* in view of *Gates, et al.*, as interconnects 201 and 210 are separated from each other by barrier layer 221 and seed layer 222 (Figure 3) and are not filled simultaneously.

Thus, Applicants respectfully maintain that *Yang, et al.* in view of *Gates, et al.* and *Naik, et al.* does not teach, suggest, or provide a reasonable expectation of success for using *Naik, et al.'s* dual damascene process to form the interconnects 201 and 210 in the structure of *Yang, et al.* in view of *Gates, et al.*

Therefore, *Yang, et al.* in view of *Gates, et al.* and *Naik, et al.* does not teach, show, or suggest a method of forming a dual damascene structure, comprising depositing a first dielectric film on a substrate, depositing an etch stop on the first dielectric film, pattern etching the etch stop to define a vertical interconnect opening and expose the first dielectric film, depositing a second dielectric film on the etch stop and the exposed first dielectric film, pattern etching the second dielectric film to define a horizontal interconnect and continuing to etch the exposed first dielectric film to define the vertical interconnect, depositing a barrier layer on the substrate, depositing a metal-containing layer on the substrate to fill both the vertical interconnect and the horizontal interconnect, planarizing the metal-containing layer and the second dielectric film, depositing a refractory metal nitride cap layer on the planarized metal-containing layer and the planarized second dielectric film by a cyclical deposition process comprising alternately pulsing a metal-containing compound and a nitrogen-containing compound to deposit the refractory metal nitride cap layer, and depositing an etch stop layer on the refractory metal nitride cap layer, as recited in amended claim 19. Applicants respectfully request withdrawal of the rejection of claim 19 and of claims 21-26, which depend thereon.

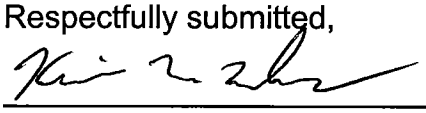
In conclusion, the references cited by the Examiner, alone or in combination, do not teach, show, or suggest the invention as claimed.

The secondary references made of record are noted. However, it is believed that the secondary references are no more pertinent to the Applicants' disclosure than the

primary references cited in the Final Office Action. Therefore, Applicants believe that a detailed discussion of the secondary references is not necessary for a full and complete response to this Final Office Action.

Having addressed all issues set out in the Final Office Action, Applicants respectfully submit that the claims are in condition for allowance and respectfully request that the claims be allowed.

Respectfully submitted,



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